ABSTRACT

Providing electrical isolation between the chipset and the memory data is disclosed. The disclosure includes providing at least one buffer in a memory interface between a chipset and memory modules. Each memory module includes a plurality of memory ranks. The buffers allow the memory interface to be split into first and second sub-interfaces. The first sub-interface is between the chipset and the buffers. The second sub-interface is between the buffers and the memory modules. The method also includes interleaving output of the buffers, and configuring the buffers to properly latch the data being transferred between the chipset and the memory modules. The first and second sub-interfaces operate independently but in synchronization with each other.